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Temperature-Dependent Photoluminescence Characteristics of InAs/GaAs Quantum Dots Directly Grown on Si Substrates *

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The first operation of an electrically pumped 1.3-μm InAs/GaAs quantum-dot laser was previously reported epitaxially grown on Si (100) substrate. Here the direct epitaxial growth condition of 1.3-μm InAs/GaAs quantum on a Si substrate is further investigated using atomic force microscopy, etch pit density and temperature-dependent photoluminescence (PL) measurements. The PL for Si-based InAs/GaAs quantum dots appears to be very sensitive to the initial GaAs nucleation temperature and thickness with strongest room-temperature emission at 400°C (170 nm nucleation layer thickness), due to the lower density of defects generated under this growth condition, and stronger carrier confinement within the quantum dots.

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Silicon photonics has been extensively researched over the past decade. However, the active photonic devices such as photodetectors and lasers have not been successfully demonstrated until recently.[1] Self-assembled III–V quantum dots (QDs) attract intense research interests and efforts due to their unique physical properties arising from the three-dimensional confinement of carriers and discrete density of states. Semiconductor III–V QD laser structures exhibit dramatically improved device performance in comparison with their quantum well (QW) counterparts, notably their ultra-low threshold current density, less sensitivity to defects and outstanding thermal stability. Therefore, integrating a high-quality QD laser structure onto silicon-based platform could potentially constitute a hybrid technology for the realization of optical inter-chip communications.[2−4]

The integration of direct GaAs heteroepitaxy on silicon is extremely challenging due to the substantial lattice and thermal expansion mismatch between GaAs and Si. The inherent high-density propagating dislocations can degrade the performance of III–V based lasers on silicon substrates. To enhance the device performance, QW dislocation filters[5] are adopted to create strain field, which bends the propagating dislocations backwards into the substrate. In addition to reducing the propagation of anti-phase domain (APD)[6] generated defects to the active layers, the determining factor is the quality of nucleation interface between III–V and Si substrates. This study is devoted to the optical research of InAs/GaAs QDs on silicon substrates under several different growth conditions.

In this Letter, we optimize the PL strengths of 1.3-μm InAs/GaAs QDs directly grown on Si substrates by varying the nucleation temperature and nucleation layer thickness at the GaAs/Si interface. Our systematical studies indicate that the InAs QDs with a 170-nm-thick nucleation layer at 400°C exhibit the strongest PL and the narrowest linewidth in the temperature range 10–300 K.

The samples were grown by solid-source III–V molecular beam epitaxy on n^+ doped (100) orientated Si substrates with 4° offcut towards the [100] plane. The initial results of the first room-temperature laser on the Si substrate were reported previously in 2011.[1,7] In this study, we further investigate the temperature-dependent optical properties of Si-substrate-based InAs/GaAs QDs in detail under different growth conditions.

Single domain GaAs can be epitaxially grown on Si substrates by setting the substrate temperature to a proper value at the beginning of the buffer layer formation, due to the fact that the surface reconstruction of the first layer on Si depends on the temperature at which the Si surface reacts with As.[7,8] The dislocation density in the GaAs buffer is also very sensitive to the initial nucleation temperature of GaAs, as discussed in the following.[8] After the de-oxidation of Si surface at 900°C for 10 min, the cooled GaAs buffer structure on Si is initialized with a 30 nm nucleated GaAs layer at GaAs/Si interface under the migration enhanced epitaxy (MEE) technique at a low growth rate of 0.1 monolayer/s. By performing a two-step growth method, an additional 970-nm-thick high-temperature (HT) GaAs is grown above at 580°C with a higher growth rate of 0.7 monolayer/s, covered by the InGaAs/GaAs QW dislocation filters.[1] The one-step growth method with a direct deposition of HT GaAs has been proved to be a particular rough technique. The two-step growth with a low-temperature nucleation followed by HT GaAs growth is the most promising technique to produce an APD-free GaAs layer on Si.[7] The growth details have been discussed in Ref. [1].

Comparing the PL spectra of the samples with low temperature MEE[9,10] at 380°C, 400°C and 420°C, the PL intensity and linewidth plots indicate that 400°C appears to be the optimum growth temperature for the initial GaAs nucleation layers, as shown in Fig. 1.

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Note that all PL measurements are performed under identical experimental arrangement with a pump power of 10 mW. As shown in Fig. 1, the highest PL intensity is obtained from the reference sample on a GaAs substrate (one with the strongest PL of InAs QDs at 1.3 µm in Ref. [11]), followed by growth of lattice-matched QDs on a Ge substrate[9,12] (red dashed line), which has a PL intensity almost similar to the reference GaAs sample.[13] It has been discussed above that 400℃ is the optimum nucleation temperature. The pink plot (sample 2) in Fig. 1 gives the highest PL intensity on the Si substrate with a low-temperature GaAs thickness of 170 nm at the optimum nucleation temperature. The other two samples (samples 1 and 3) grown at different nucleation temperatures (380℃ and 420℃) with identical thickness show an obviously weaker PL intensity due to rougher GaAs/Si interfaces. Furthermore, in comparison, different thicknesses of low-temperature GaAs buffer are studied as sample 4 with 70 nm and sample 5 with 270 nm at the optimized identical nucleation temperature (400℃). It can be observed that there is a strong degradation in PL intensity for sample 4, which has a thinner 70 nm low-temperature GaAs buffer layer. A thinner low-temperature buffer has a significant impact on the surface morphology of high temperature GaAs buffer grown above, therefore, further influences the optical properties of active layers. The thicker 270 nm low-temperature GaAs layer (sample 5 in Fig. 1) will also degrade the quality of grown GaAs, as it was grown at a temperature lower than the optimized temperature for GaAs and thus tends to create additional defects.

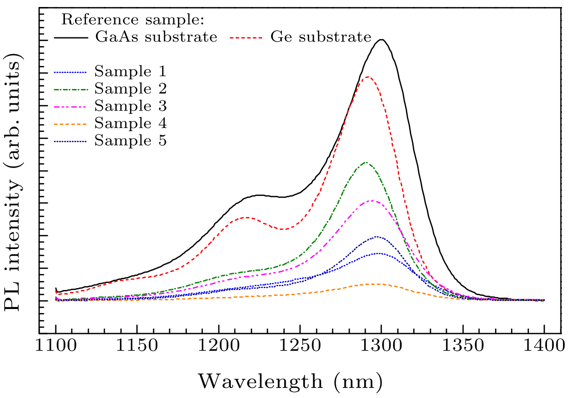

Fig. 1. Room-temperature PL spectra of InAs/GaAs QDs grown on GaAs and Si substrates. For Si substrates, there are five samples under different growth conditions.

We study the effects of GaAs nucleation temperature and thickness on the PL intensity of InAs QDs, and the correspondent atomic force microscopy (AFM) images of uncapped InAs QDs under different growth conditions are listed in Fig. 2. The AFM images are the laser structures in which the growth was terminated immediately after the dot deposition, where the InAs QDs remains uncapped with an approximate dot density of 4.3×10^{10} cm^2 for Fig. 2(b) with the least amount of defects. It can be clearly observed that there are defected dots existing in the AFM images, which are the accumulated InAs clusters due to strain release. The quantum dots are relatively small to be observed in the 5×5 µm^2 AFM images, where only large defect dots can be observed. The defect-dot densities of 9.64×10^8, 2.68×10^8, and 4.92×10^8 cm^{-2} are obtained for samples a, b and c with the initial GaAs layer nucleated at 380, 400, and 420℃, respectively. By occupying the optimum nucleation temperature at 400℃, samples d and e with different thicknesses of initial low-temperature GaAs (70 nm and 270 nm) have the corresponding defect-dot densities of 1.63×10^9 and 9.32×10^8 cm^{-2}.

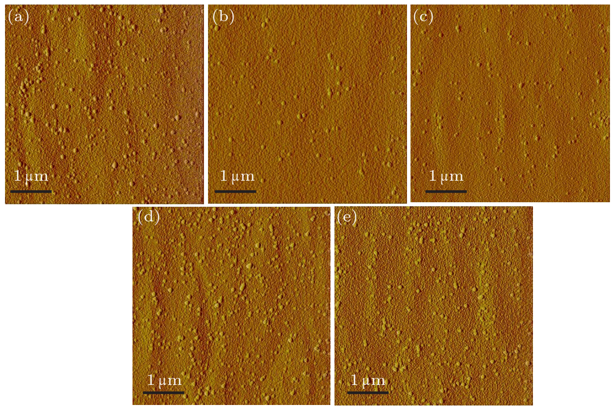

Fig. 2. The 5×5 µm^2 AFM images of surface InAs QDs under different growth conditions: 170-nm-thick nucleation layer at (a) 380℃, (b) 400℃, (c) 420℃, (d) 70-nm-thick and (e) 270-nm-thick nucleation layer at 400℃.

Figures 2(a)–2(c) show the nucleation temperature optimization, which give the optimum nucleation temperature at 400℃ with the least amount of defected dots. Apart from the investigations of GaAs nucleation temperature on Si substrates, there are further studies carried out on the thickness of initial low-temperature GaAs on Si. By using the optimized nucleation temperature, the low-temperature GaAs buffer layers are grown with two other different thicknesses, as shown in Figs. 2(d) and 2(e). The sample in Fig. 2(d) with the thinnest low-temperature GaAs buffer layer at 70 nm has the highest defect-dot density, which corresponds to the weakest PL intensity in Fig. 1.

Of considerable significance is that the PL intensity of the InAs/GaAs QD ground-state transition on Si is strongly dependent on the growth temperature of the initial GaAs nucleation layer.[7] The strongest PL intensity for InAs/GaAs QDs on Si substrates is obtained from the sample with initial GaAs growth at 400℃, and it is more than half the one of InAs QDs grown on GaAs substrates. It should be mentioned that the InAs QDs grown on GaAs substrates were grown under optimized conditions and represents very high optical quality as the QD laser diode based on identical growth parameters gives an extremely low $J_{\rm th}$ of 17 A/cm^2 and high output power over 100 mW at room temperature.[14]

The AFM results show a direct correlation between defect-dot density and room-temperature PL intensity, which is strongly dependent on the nucleation temperature and thickness of the low-temperature GaAs buffer layer at the GaAs/Si interface. In addition, the defect dot densities are in line with the room-temperature PL spectra. The strongest room-temperature PL occurs on the InAs/InGaAs QD sample on Si at 400℃ nucleation temperature with 170 nm thickness of the buffer layer, which has the lowest defect dot density.

Table 1. EPDs of the laser structures on Si with different growth temperatures.

GaAs/Si	380℃	400℃	420℃
Etch pit density	1.03×10^7 cm^2	6.03×10^6 cm^2	8.17×10^7 cm^2

An etch-pit density (EPD) test is introduced to further verify the above results as listed in Table 1. All the three samples are etched 1.5 µm down from the surface to determine interface-generated threading dislocation (TD) densities, where the etchant used for the EPD delineation is a mixture of H_3PO_4, H_2O_2, and H_2O (in a 1:1:3 ratio).[15] From Table 1, it can be observed that the sample grown at 380℃ has 1.7 times higher defect-density than the optimized growth at 400℃, where the sample grown at 420℃ is even worse with 13.55 times higher. This EPD comparison explains the intensity differences in the room-temperature PL correspondingly as shown in Fig. 1, where the room-temperature PL spectra of all the three samples are investigated, excited with a low laser power approximately 5 mW. Therefore, it is verified that the defect density within GaAs buffer layers is strongly dependent on the GaAs nucleation temperature. The relatively lower temperature at 380℃ generates significantly more defected dots than the other two due to its poor material quality and high TD density at low temperature nucleation. At 400℃, the higher temperature has provided atoms with much higher mobility to move around to eliminate surface defects. However, excess thermal energy can also induce strong atomic movement, and therefore can damage the sample surface, which explains the PL degradation at 420℃. Therefore, we can conclude that the EPD results match up with the surface defect dot densities obtained from AFM images.

Temperature-dependent PL spectra ranging 10–300 K were further studied for all the InAs/GaAs QDs grown on Si substrates. All the samples were mounted on a flat copper plate within the cryostat under accurate temperature control. A solid-state laser, emitting at 532 nm, was used as the excitation source; the emitted radiation from the material is detected by a TE-cooled Ge detector. A 1/4 m Newport monochromator with a focal length of 260 mm is used here. Lastly, a fixed laser power of 30 mW was here used for temperature-dependent PL measurements for all the samples.

To further investigate the mechanisms of the influence of temperature and thickness of the GaAs nucleation layer on the optical properties of Si-based InAs/GaAs QDs, the integrated PL intensity (IPLI)[16] between 10 and 300 K are analyzed. With a low laser power excitation, only the ground-state emission appears in the PL. Figure 3 shows the Arrhenius plot of the IPLI for three different growth temperatures of the GaAs nucleation layer. The variation of IPLI data with temperature can be described by the generic empirical relationship[16,17]

$$IPLI = \frac{I_0}{1+\sum_i C_i \exp\left(\frac{E}{kT}\right)}, \tag{1}$$

where E is the thermal activation energies (TAE) for loss mechanisms active in certain temperature ranges, k is the Boltzman constant, T is the temperature, and I_0 and C are fitting constants.[17]

These temperature-dependent variations of IPLI could be understood in terms of the recombination rates and the geometric dimensions of the dots. Note that the IPLI has a quenching threshold temperature for all the samples.[18] From Figs. 3(a) and 3(b), the IPLI plots remain almost constant until the quenching threshold temperature, and then decreases gradually until room temperature. The IPLI starts to quench at the point where the carrier capture time into QDs is becoming longer than the carrier lifetime in the barrier, which indicates that there are more carriers escaped than captured. Thus it can be clearly found that the quenching occurs due to the losses in the barrier at higher temperature. Here the carrier lifetime in the barrier is strongly dependent on the non-radiative recombination center, i.e., the concentration of defects. It can be observed in Fig. 3(a) that the IPLI exhibits the highest quenching temperature of 77 K for the optimized growth at 400℃, which indicates less thermal escape due to the reduction in defect density.[19] Hence, the carrier lifetime in the barrier is longer, which explains the persistence of IPLI to a higher temperature. The highest TAE is found in 81R2 with a value of 101.74 meV, which means the highest required energy for carriers to escape from the active region. In comparison, the other samples with lower TAE have correspondingly weaker carrier confinement at the presence of incoming thermal energies as shown in Figs. 3(a) and 3(b). In other words, the sample with higher TAE indicates a lower sensitivity to temperature. It is also verified in Table 1 that the optimized sample at 400℃ has a much lower defect density than both higher and lower growth temperatures, which directly determine the highest TAE among all the samples. Therefore, the high quality growth of the GaAs buffer layer at 400℃ nucleation provides a much higher carrier lifetime in the barrier material, leading to the highest room-temperature IPLI among the three samples.

Furthermore, these three samples in Fig. 3(b) are grown at the same nucleation temperature of 400℃, but with different low-temperature GaAs thicknesses of 70 nm, 170 nm and 270 nm. The sample 81R2, under the optimum growth condition, has shown the strongest IPLI all over the whole temperature range, followed by 82R2. Although the IPLI starts dropping dramatically above 77 K, the IPLI still remains persistent at a high level, which is attributed to the increase of the oscillator strength due to additional lateral confinement in QDs compared with conventional quantum wells. The reduction in IPLI is normally attributed to thermal escape into the barrier material (InGaAs/GaAs) followed by non-radiative recombination in the barrier. Therefore, in this case, the IPLI differences among the three samples in Fig. 3(a) are mainly caused by the defect density difference due to the nucleation temperature. Additionally, by studying the variation of the nucleation layer thickness as shown in Fig. 3(b), either thicker or thinner nucleation layer can lead to the generation of TDs, further degrading the IPLI. Clearly, the sample 81R2 grown at 400℃ with a 170-nm-thick low-temperature GaAs buffer layer has the least amount of TDs, which gives the highest IPLI over the temperature range of 10–300 K.

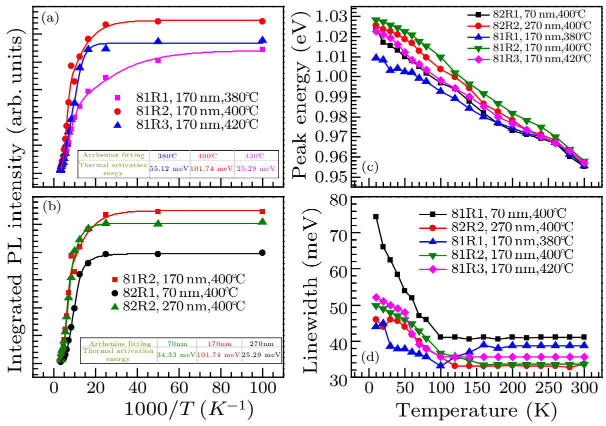

Fig. 3. The Arrhenius plots of IPLI of InAs QD samples on Si with (a) three different nucleation temperatures of 380℃, 400℃ and 420℃, (b) three different thicknesses of nucleation layers, (c) peak energies, and (d) linewidths of temperature-dependent PL spectrum versus temperature.

In Fig. 3(c), the percentage of change in the energetic position of PL peak emission remains almost linear for the best two samples (81R2 and 82R2) over the temperature range of 10–300 K. Due to the degradation of QDs quality under other growth conditions, the PL peak positions in energy (81R1, 81R3, 82R1) appear to fluctuate with the increasing temperature.

Lastly, in Fig. 3(d), the full-width-at-half-maximum (FWHM), or linewidth of the PL spectrum varies between 33 meV to 37 meV for sample 81R2 in the temperature range of 77–300 K has the least variation of 12% and the narrowest room-temperature linewidth among all the samples. At lower temperature, the FWHMs of all the samples substantially increase due to the effect of spectrum broadening due to the additional emission from small quantum dots.[20] At high temperature, the dominant quantum dots with high localization energy will be preferentially occupied by the carriers, resulting in a narrowing of FWHM. In comparison, samples grown at 380℃ and 420℃ have relatively larger variations of 20% and 25%. Sample 81R1 has the strongest FWHM variation for the temperature-dependent PL, due to the fact that the appearance of the emission from small QDs at low temperatures (below 200 K) has broadened the FWHM of the spectrum. At room temperature, the sample grown at 400℃ (81R2) shows the narrowest linewidth of 33.22 meV. Both the samples (82R1 and 82R3) grown at 380℃ and 420℃ have broader linewidths at 39.28 meV and 35.77 meV.

By having the optimum nucleation temperature at 400℃, 82R1 with a thinner 70-nm GaAs buffer has the broadest linewidth of 41.98 meV at room temperature. The sample 82R2 with thicker 270-nm GaAs buffer shows a very narrow linewidth similar to 81R2. Therefore, in the comparison of FWHM of PL spectra, 81R2 and 82R2 with the same nucleation temperature, but different thicknesses of low-temperature GaAs buffer at 170 nm and 270 nm, respectively, have similar performance in FWHM optimization. Such a small variation in the FWHM of the PL emission indicates the uniformity of QD sizes for the sample 81R2 grown with a nucleation thickness of 170 nm at 400℃.

In summary, the growth conditions of the GaAs nucleation layers on Si substrates have been extensively studied by analyses of temperature-dependent PL spectra, where a 170-nm-thick nucleation layer at 400℃ is found to be the optimum growth condition for Si substrates. The lowest EPDs, least amount of defect dots and strongest PL intensity, are achieved simultaneously to suggest that the high-performance laser devices should be fabricated under this optimum condition. The correlation between the optical performance of InAs/GaAs QDs on Si and directly grown GaAs/Si interface quality has been fully understood for the first time.

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