

Monolithic Growth of Ultrathin Ge Nanowires on Si(001)

J. J. Zhang,^{1,*} G. Katsaros,^{1,5} F. Montalenti,² D. Scopece,² R. O. Rezaev,^{1,6} C. Mickel,⁴ B. Rellinghaus,⁴
L. Miglio,² S. De Franceschi,³ A. Rastelli,^{1,5} and O. G. Schmidt¹

¹*Institute for Integrative Nanosciences, IFW Dresden, D-01069 Dresden, Germany*

²*L-NESS and Department of Materials Science, University of Milano-Bicocca, I-20125 Milano, Italy*

³*SPSMS, CEA-INAC/UJF-Grenoble 1, F-38054 Grenoble Cedex 9, France*

⁴*Institute for Metallic Materials, IFW Dresden, D-01069 Dresden, Germany*

⁵*Institute of Semiconductor and Solid State Physics, University Linz, A-4040 Linz, Austria*

⁶*Laboratory of Mathematical Physics, Tomsk Polytechnic University, Lenin Avenue 30, 634050 Tomsk, Russia*

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Self-assembled Ge wires with a height of only 3 unit cells and a length of up to 2 micrometers were grown on Si(001) by means of a catalyst-free method based on molecular beam epitaxy. The wires grow horizontally along either the [100] or the [010] direction. On atomically flat surfaces, they exhibit a highly uniform, triangular cross section. A simple thermodynamic model accounts for the existence of a preferential base width for longitudinal expansion, in quantitative agreement with the experimental findings. Despite the absence of intentional doping, the first transistor-type devices made from single wires show low-resistive electrical contacts and single-hole transport at sub-Kelvin temperatures. In view of their exceptionally small and self-defined cross section, these Ge wires hold promise for the realization of hole systems with exotic properties and provide a new development route for silicon-based nanoelectronics.

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As miniaturization in complementary metal oxide semiconductor transistors proceeds and approaches the atomic scale, the reliability and reproducibility of transistors become increasingly difficult because of random fluctuations in the number of dopants included in the active device. Furthermore, as dimensions shrink, surface defects present in top-down etched structures become more and more detrimental.

In this context, Ge-based semiconducting nanowires (NWs) are attracting great interest [1–3]. Doping-free Ge/Si core-shell NWs with diameters of 20 nm were used to fabricate field-effect transistors that showed performances comparable to state-of-the-art devices fabricated by conventional lithographic top-down processes [2,4]. Outstanding electrical properties, such as ballistic conduction up to length scales of several hundred nanometers, were reported in such core-shell NWs [5]. Recently, atomic-scale NWs could be fabricated on Si(001) and Ge(001) surfaces using a lithography technique based on scanning tunneling microscopy and a gaseous dopant source [6,7]. With such wires Ohm's law was observed to hold at the atomic scale [7], making them suitable as interconnects. While miniaturization poses problems for applications, it opens up many possibilities for investigating fundamental physics. Indeed transport through single dopants has been observed [8,9] and the realization of spin qubits has become possible [10]. A very recent proposal [11] has further suggested that *ultrathin, strained* Ge NWs can support helical modes, which renders them appealing for realizing spin filters [12], Cooper-pair

splitters [13] and for observing exotic quantum states, like Majorana fermions [14–17].

Ge NWs are commonly obtained by vapor-liquid-solid growth, in which a metallic catalyst nanoparticle initiates and sustains the growth of a wire out of the substrate plane [1]. The use of metallic catalysts, however, introduces metal contamination [18], making the integration with microelectronics technology rather problematic. It is also a formidable challenge to transfer and arrange these vertically grown NWs to an adequate substrate for device fabrication.

Alternatively, already in 1993, Tersoff and Tromp [19] suggested that catalyst-free, ultrathin Ge “quantum wires” with large built-in strains could be grown epitaxially on flat Si substrates. In this letter, we show that such types of wires can indeed be obtained by a self-assembled process implemented in a solid-source molecular beam epitaxy (MBE) growth setup. The self-assembly of the Ge NWs is achieved through a surprisingly simple procedure consisting of the epitaxial deposition of a Ge layer on a Si(001) substrate followed by thermal annealing at appropriate temperatures. Compared to NWs grown by catalytic methods [1–3], the catalyst-free Ge NWs presented here exhibit an outstanding uniformity in their lateral size, they lie horizontally along well-defined crystallographic directions (either [100] or [010]), and they are monolithically integrated into the silicon substrate. Our theoretical calculations show that the formation of {105} facets plays a key role in determining the stability and uniformity of the wires. The successful realization of good electrical contacts to individual wires and the observation of

single-hole transport make them a promising system for realizing both ultrasmall *p*-type Ge transistors on Si and novel quantum devices.

The Ge NWs were grown by MBE at a base pressure of 5×10^{-11} mbar. We initially deposit 4.4 monolayers (ML) of Ge to form a pseudomorphically strained two-dimensional layer, known as the wetting layer (WL), with a growth rate of 0.04 ML/s at a substrate temperature of 570 °C. The deposited Ge amount is slightly smaller than the critical thickness of 4.5 ML for the formation of three-dimensional (3D) Ge islands, referred to as “hut clusters” [20–25]. After Ge deposition, the substrate temperature is kept at nominal 560 °C for different time durations. During this *in situ* annealing, 3D islands appear and evolve into long wires via anisotropic growth along either the [001] or the [010] crystallographic direction, as shown in Fig. 1(a). This finding indicates that, for the chosen amount of deposited Ge, the WL is metastable against 3D island formation [26]. The length of the wires is typically already a few hundreds of nanometers after 1 h annealing and reaches the micrometer scale in 3 h. Further annealing

produces only a limited increase in their length, as shown in Fig. 2(a). This may be attributed to the fact that, as Ge moves into the wires, the WL is consumed leading to gradual reduction of the growth rate due to the depletion of the Ge supersaturation [24]. As seen from Fig. 1(a) the wires are highly uniform in height and width. A statistical analysis performed on NWs longer than 80 nm shows an average height h of 1.86 nm (about three unit cells) with a remarkably low standard deviation (0.14 nm). The NWs have the triangular cross-section characteristic of hut clusters [Fig. 1(d)], with {105} side facets forming an angle $\theta = 11.3^\circ$ with the substrate plane and resulting in an average base width $b = 2h/\tan\theta = 18.6$ nm. This is confirmed by cross-sectional transmission electron microscopy (TEM) as shown in the inset of Fig. 1(d). Figure 2(b) shows the histograms of height distribution of all nanostructures including short hut clusters and pyramids [as seen in Fig. 1(a)] after 1, 3, and 12 h annealing. Different from the length, the height distribution does not show significant variations during annealing, indicating the wires grow by increasing only their length [24]. In addition, pyramids and hut clusters usually have a larger height (> 2 nm), compared to the wires, suggesting that islands with a large height are difficult to elongate.

The wire density can be controlled simply by the amount of the initially deposited Ge. By decreasing it, the amount of metastable Ge is correspondingly decreased, resulting in a

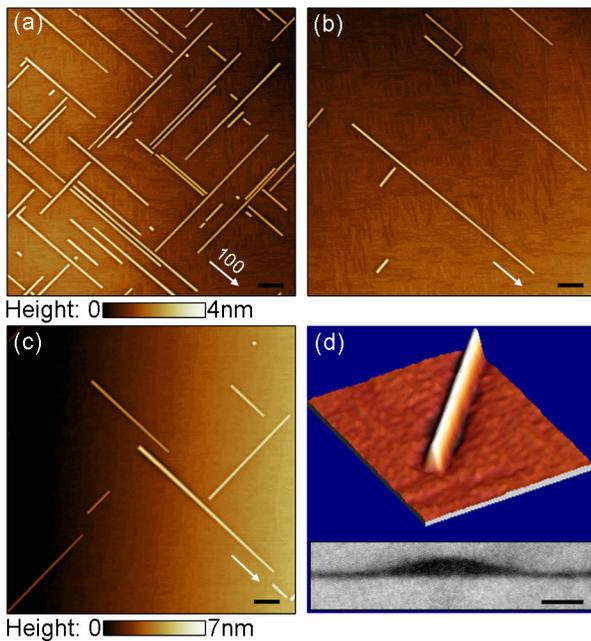


FIG. 1 (color online). Atomic force microscopy (AFM) images of Ge wires forming on Si(001) substrates after 12 h annealing. Atomic terraces are parallel to the (001) plane and atomic steps on the WL are well visible. (a) High and (b) low density of Ge wires on Si(001) with a nominal miscut angle of less than 0.05° . (c) Tapered Ge wires on Si(001) with a nominal miscut angle of less than 0.5° . The wires grow laterally along either of the two $\langle 100 \rangle$ directions as indicated by the arrows and their surface is composed of four {105} facets. Scale bar: 200 nm. (d) 3D AFM image of an individual Ge wire. The inset is a cross-sectional TEM image of the Ge wire capped with Si at 300 °C, showing a sharp Si/Ge interface and an inclination angle of 11.3° between {105} facets and the substrate plane. Scale bar: 5 nm.

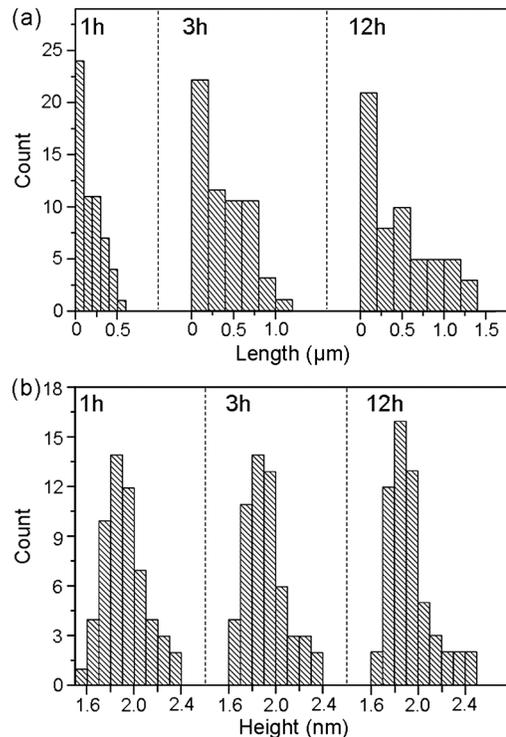


FIG. 2. Histograms showing the length distribution (a) and the height distribution (b) of Ge nanostructures (including wires, pyramids and hut clusters) for different annealing times at a substrate temperature of 560 °C.

reduced island nucleation rate [27]. Under these conditions the wire density drops [Fig. 1(b)], but the maximum wire length increases up to $L \sim 2 \mu\text{m}$, which corresponds to a length L to height h ratio as large as ~ 1000 . By increasing the initial Ge amount, a larger density of comparatively shorter wires is obtained (see Supplemental Material [28]). We attribute this observation to two factors: (i) an initially larger island density leads to an increased probability of “collisions” between growing wires and consequent interruption of wire growth due to strain repulsion [29]; (ii) the Ge material available for each wire decreases, so that even relatively isolated wires cannot grow too long.

We find that the Ge wires have a constant height (width) as long as they grow on the same atomic terrace. When their length extends over several terraces, we observe the top ridge of the wires to remain parallel to the (001) plane, at least for moderate local miscut angles. In other words, as a wire crosses an atomic step on the underlying substrate its height will increase or decrease by 0.14 nm (i.e. the height of an atomic step). This implies that by choosing the morphology of the Si surface prior to growth, the size of the wires can be tuned at the atomic-scale. On substrates with larger terraces, which may be obtained as in Ref. [30], we expect all the wires to have a constant height (width). On substrates with smaller terraces, tapered wires are instead observed [Fig. 1(c)].

The Ge wires do not consist of pure Ge due to the Si-Ge intermixing taking place during Ge deposition and the subsequent annealing process. Although the ultrasmall dimension of the wires does not allow us a more detailed determination of the composition, our selective wet chemical etching in H_2O_2 solution shows that the Ge content is higher than 65% even at the base which is known to have the lowest Ge content [28].

Let us now show that there exists a strong thermodynamic driving force stabilizing long {105}-faceted wires. We evaluate the energy difference ΔE between a wire on an N -layer thick WL, and a configuration where the same material is instead spread on the WL, creating a region with $N + 1$ layers. Here all parameters are quantified by considering pure Ge. Because of the large aspect ratio L/b of interest, the energy change can be computed by disregarding wire terminations (see inset of Fig. 3, and discussion in the Supplemental Material [28]). In this way we consider directly mature huts neglecting the first seeds and their initial stages of growth and elongation. Since this processes are likely to involve atomic-scale effects [21–25], further investigations are needed to capture their physics and evolution, but this is out of the scope of the present work. By taking into account elastic-energy relaxation, surface-energy differences, and wire edge energies, simple calculations lead to [28]:

$$\Delta E = V \left[\Delta\rho_{\text{eff}} + \frac{4}{b \tan\theta} \Delta\gamma + \frac{4\Gamma}{b^2 \tan\theta} \right], \quad (1)$$

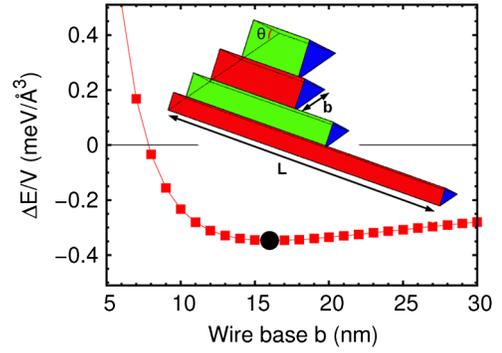


FIG. 3 (color online). The energy difference ΔE (divided by volume) between a wire and a 2D configuration of equal V , as obtained using Eq. (1), is plotted vs base width b . The inset illustrates the structures used in the model: truncated wires with only two {105} facets. Points along the curve in the plot represent wires of different length but same volume, as sketched in the inset. The black filled circle indicates the base width b_{min} , corresponding to the minimum-energy configuration. b_{min} is volume independent.

where V is the wire volume, Γ the total energy associated with edges connecting adjacent facets, and $\Delta\rho_{\text{eff}} = \Delta\rho_{\text{el}} + (1/h_1)[\gamma_{\text{WL}}(N) - \gamma_{\text{WL}}(N + 1)]$, i.e., the sum of the elastic energy (per unit volume) lowering, provided by the wire geometry and the surface-energy change obtained by adding the $(N + 1)$ th layer (with height h_1) to the WL [28,31]. Finally, $\Delta\gamma = \gamma_{\text{hut}} \sec\theta - \gamma_{\text{WL}}(N)$, where γ_{hut} is the surface energy (per unit area) of the wire. $\Delta\rho_{\text{el}}$ was quantified by finite element method (FEM) calculations, surface energies were extracted from *ab initio* calculations [28,32], while $\Gamma = 370 \text{ meV}/\text{\AA}$ accounts for wire edge energies, as obtained from experimental fitting in Ref. [33]. To mimic the experiment, we set $N = 4$. A plot of $\Delta E/V$ vs b , shown in Fig. 3 demonstrates that (i) There exists a “magic” base width $b_{\text{min}} \approx 2\Gamma_{\text{hut}}/(-\Delta\gamma)$, minimizing the energy of a wire at fixed volume, and (ii) wire formation is energetically favorable vs WL thickening, as indicated by the corresponding negative value of ΔE . These results are a direct consequence of the very low surface energy of Ge{105} under compressive strain [33,34], $\Delta\gamma \approx -4.5 \text{ meV}/\text{\AA}^2$, implying that the driving force for wire formation is the reduction of surface energy, rather than strain relaxation (which is 1 order of magnitude smaller [28]). This energy gain is however counterbalanced by the edge energy, dominating at small b values, and resulting in a favored width. Remarkably, the theoretical estimate $b_{\text{min}} \approx 16.3 \text{ nm}$ is within about 15% of the experimentally observed value. The presence of a V -independent minimum in the $\Delta E/V$ curve, explains not only the sharp distribution of NW cross-sectional sizes but also the tendency towards “infinite” elongation. In addition, one notices an asymmetric behavior in terms of $\Delta E/V$ vs b around the minimum. For $b < b_{\text{min}}$, the quantity $\Delta E/V$ increases much faster than for $b > b_{\text{min}}$. This leads to the prediction that it is

energetically easier to increase the cross section of a wire rather than decrease it. This is exactly what we observe in our experiments (Fig. 1): The smaller ends of tapered wires have a rather uniform width of about 16 nm, which is very close ($\Delta b/b_{\min} \sim 15\%$) to the experimentally determined b_{\min} (18.6 nm). In contrast, the larger ends have a broad width distribution extending up to 40 nm [Fig. 1(c)], corresponding to ($\Delta b/b_{\min} \sim 115\%$). We therefore believe that on stepped terraces the wires preferentially grow by crossing down steps rather than up steps. We conclude that the model provides an excellent explanation of the main experimental findings.

After over two decades of research on the Ge/Si epitaxial system, it may seem surprising that the nanowire growth method presented above has not been reported before. In fact, although conceptually simple, this method requires certain growth conditions to be met. For instance, any initially crowded environment (in terms of critical nuclei) would not allow the observation of micronlong wires, because of self-blocking (due to strain repulsion) and/or coarsening. With this respect, the annealing of an initially

flat WL with proper thickness seems to be a key to reduce the density of mobile species leading to clustering. A too large amount of Ge or too high temperature during growth or subsequent annealing would again increase such density (the thicker the WL, the weaker the atomic bonds [31]). On the other extreme, too low temperature and/or too thin WL would simply suppress both wire nucleation and elongation through surface diffusion.

In view of their extremely small and uniform cross section, the Ge NWs reported here are excellent candidates for the realization of novel electronic devices. To this aim, a new set of samples were grown in which the Ge NWs were covered by a few-nm-thick Si cap layer to create core-shell structures. The Si cap layer was grown at a relatively low temperature of 300 °C in order to reduce intermixing and obtain a sharp Si/Ge interface, as seen from the TEM image in Fig. 1(d). FEM calculations show that the Ge NWs are partially strained without the Si cap [28] and become almost fully strained to the Si lattice in the growth plane with a 2 nm-thick Si cap [Fig. 4(a)]. Three-terminal, field-effect devices were fabricated out of individually

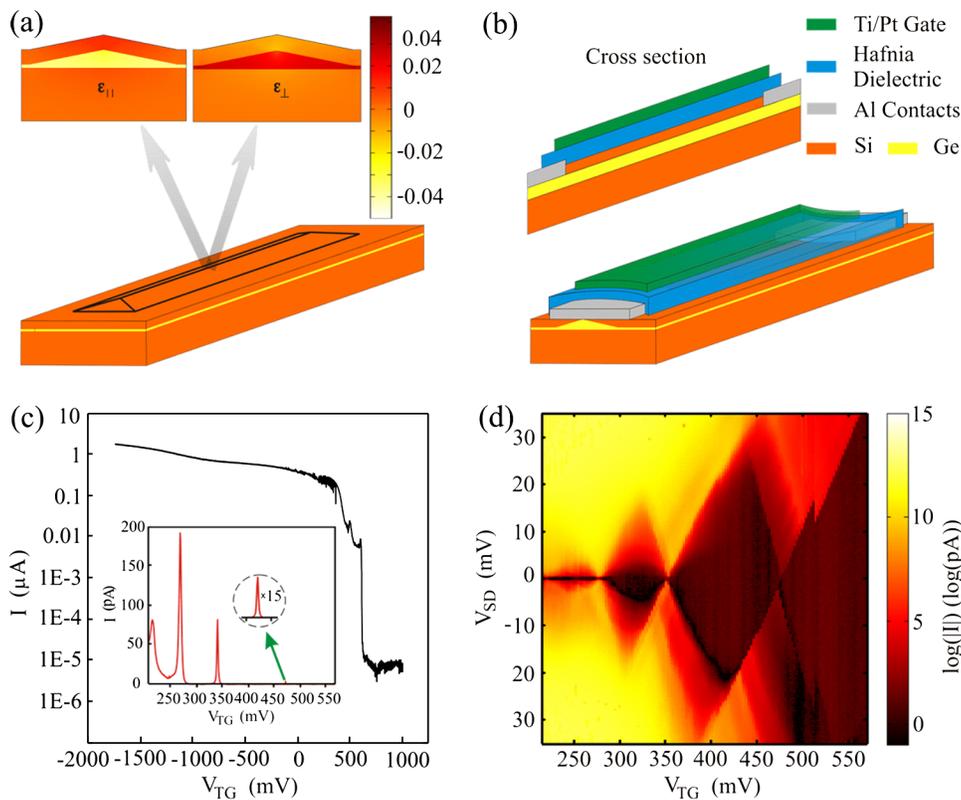


FIG. 4 (color online). (a) Schematic of a Ge wire capped with a 2 nm-thick Si cap. The in-plane (left) and out-of-plane (right) components of the strain distribution are shown. (b) Schematic of a device showing the Ge wire contacted by Al electrodes (gray), covered with a ~ 10 nm hafnia layer (blue) and a layer of Ti/Pt (10/90 nm) acting as a top gate (green). The top left scheme shows a cross-section along the wire. (c) I vs V_{TG} at $V_{SD} = 75$ mV. The device can be switched off at about 600 mV while currents higher than $1 \mu\text{A}$ can flow through the wire at high negative gate voltages. For $V_{SD} = 0.25$ mV (inset), characteristic peaks originating from Coulomb blockade can be observed. (d) $|I|$ vs V_{TG} and V_{SD} , revealing Coulomb diamonds and charging energies as high as 25 meV. The conductance throughout the plot is reduced at zero bias due to the superconducting properties of the Al electrodes. This can be seen more clearly in a second device [28].

contacted core-shell wires [Fig. 4(b)] [28]. The metallic contacts were deposited close to each other, defining a 30–50 nm wide channel. At room temperature, these devices are shunted by a significant leakage current through the Si substrate. Therefore, their basic electrical properties were only studied at low temperature using a ^3He refrigerator. Figure 4(c) shows a representative measurement of the source-drain current (I) as a function of the top-gate voltage (V_{TG}) at 260 mK. The $I(V_{\text{TG}})$ dependence confirms the p -type character of the NWs, originating from the type II band alignment between Si and Ge and from the pinning of the contact Fermi level near the Ge valence-band edge. The device can be tuned from a fully pinched-off state for $V_{\text{TG}} > 0$, to a relatively low-resistance state (40 k Ω) for $V_{\text{TG}} < 0$. Remarkably, I as high as a few μA , corresponding to current densities of 10^7 A/cm 2 , could be driven through the Ge NW. At small source-drain voltage (V_{SD}), the $I(V_{\text{TG}})$ characteristic exhibits a sequence of narrow peaks as shown in the inset of Fig. 4(c). From a 2D plot of $|I|$ as a function of V_{TG} and V_{SD} , shown in Fig. 4(d), we ascribe these peaks to single-hole transport occurring at the degeneracy between the consecutive charge states of a *single* quantum dot, created between the source and drain metal contacts. In each of the diamond-shape regions, transport is blocked by a Coulomb energy barrier and the quantum dot holds a well-defined, integer number of holes.

The above results lay the ground for a range of fundamental studies and device applications at low temperature. The operation of Ge-NW devices may be further extended to room temperature by replacing the Si substrate with silicon on insulator (SOI) substrates with a very thin Si surface layer. In this perspective we have successfully grown Ge NWs on SOI substrates with a 35-nm-thick Si surface layer [28], paving thus the way towards the realization of devices operating at room temperature.

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*j.zhang@ifw-dresden.de

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